低リップル・長パルス高電圧電源を実現するための回路方式

CIRCUIT METHOD FOR REALIZING LOW RIPPLE AND LONG PULSE HIGH VOLTAGE POWER SUPPLY

郭子毅#), 須貝太一, 徳地明, 江偉華
Ziyi Guo#), Taichi Sugai, Akira Tokuchi, Weihua Jiang
Nagaoka University of Technology

Abstract

This research proposes a pulse power supply circuit method that can output relatively long pulse and low ripple voltage waveforms for the purpose of accelerator application. In this study, firstly, based on the theoretical calculation and the principle of the circuit, the determination method of the parameters of each component in the circuit is discussed. Then, based on the standard of the pulsed power generator for klystron currently on the market, the parameters of each element of the test circuit were set, and the simulation was performed using LT Spice. After confirming that this circuit is theoretically feasible by simulation, we made a test circuit of one unit and evaluated its operating characteristics. As the result of conducting a demonstration experiment at a switching frequency of 50 kHz, it was confirmed that the ripple at an output voltage of 400 V, an output current of 80 A, and a pulse width of 0.5 ms was about 1.5%. From the experimental process of this research, it was confirmed that there are problems that the magnetic field coupling phenomenon due to the current change in the charging circuit and the discharge capacity discharge rate affect the output in the task of further reducing the ripple. Further, since the circuit increases and decreases periodically, there is a possibility that the ripple can be further reduced by controlling the phase between the multi-stage pulse power circuits.

INTRODUCTION

The International Linear Collider (ILC) will use a 10 MW multi-beam klystron as the microwave source. As shown in Table 1, the power supply of the multi-beam klystron is required to have a high-precision and long-pulse power supply as compared with a general high-voltage pulsed power generator. The output pulse is required to have a voltage of 120 kV (± 0.5%), a current of 140 A, a pulse width of 1.7 ms, and a repetition rate of 5 pps. When a pulse transformer is used as the power supply, it is necessary to use a large core, which increases both the size and cost and slows down the start-up. As a method that does not use a pulse transformer, a method that uses a Marx generator is useful [1-3]. The ILC plan shows us the demand of the next generation accelerator for long pulse and low ripple pulsed power generator, so it is very meaningful to develop a pulsed power generator that can meet such requirements. This may not be for the needs of the ILC plan, but to adapt to the development of accelerators. Therefore, We propose a new pulsed power circuit to realize the requirements of long pulse and low ripple as an another choice.

s195081@stn.nagaokaut.ac.jp

Table 1: Specification of Pulsed Power Supply [4]

Output Voltage	-120 kV
Output Pulse Flat-top	< ±0.5 %
Output Current	140 A
Pulse Width (flat-top)	1.65 ms
Pulse Repetition Frequency	5 Hz
Rise time and Fall time	< 0.1 ms
Energy deposited into klystron during a gun spark	< 20 J

CIRCUIT METHOD FOR REALIZING LOW RIPPLE AND LONG PULSE HIGH VOLTAGE POWER SUPPLY

Structure and operation of the proposed circuit

Figure 1 shows the circuit of pulsed power generator of one unit proposed by us. The idea of the circuit is to discharge every two stages alternately in Marx pulsed power generator, and then charge one stage during the period when it is not discharged, so as to compensate for the voltage drop caused by capacitor discharge. In the circuit diagram, we regard the two-stage Marx power supply circuit and their common charging circuit as the pulse power circuit of one unit proposal. The common charging circuit is composed of charging capacitor, switch, current limiting inductance and Compensation Diode. The charging switch uses PWM control signal to ensure that the amount of charge consumed by C1 and C2 each discharge is accurately supplemented in each charging. The charging and discharging process of the circuit is also shown in Fig 1. The green line indicates the charging process, and the red line indicates the discharging process. The capacitors C1 and C2 are continuously discharged and charged alternately, and the current waveform of long pulse and low ripple is output to the load. The magnitude of the ripple is theoretically determined by the voltage drop caused by each discharge of C1 and C2. Figure 2 is the waveform diagram of the theoretical output voltage.

The technical topics of the circuit system include maintaining the continuity and stability of the output voltage

during capacitor interactive discharge, and controlling the speed and accuracy of pulse charging.

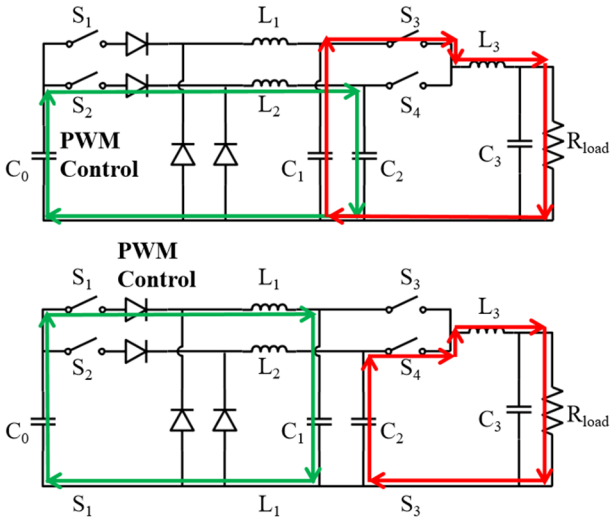

Figure 1: Circuit diagram of the proposed pulsed power circuit of one unit.

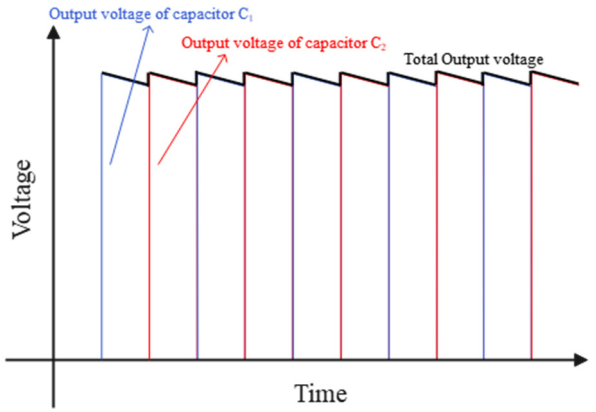

Figure 2: Theoretical output of the proposed circuit.

Structure and operation of the proposed circuit

1) Design of capacitance C1 and C2

In general, the capacity of capacitor C1 and capacitor C2 and the switching frequency are determined by the size of the target ripple. Theoretically, the ripple is the ratio of the voltage drop generated by each discharge of the capacitor to the output voltage. It can be predicted that there are more factors causing larger ripple in practice, so the theoretical ripple size in the design stage is better than the target ripple. For example, when the ripple size below ± 1% is required, the voltage drop caused by each discharge of the capacitor shall be less than 2% of the output voltage. If the design voltage drop is 1%, the relationship between the capacitance and the switching frequency can be determined by the following formula.

$$(1-1\%)U_0 = U_0 \times e^{-\frac{1/f}{RC}} \tag{1}$$

Where U0 is the voltage at the beginning of each discharge of C1 and C2, f is the switching frequency, R is the size of load resistance, and C is the capacity of C1 and C2. When the switching frequency is high, the capacity of the required capacitor can be reduced, but it is still necessary to ensure that the charging can be completed during the non discharge period of the capacitor, which requires the charging switch to bear more current.

2) Design of charging circuit

Compared with the design of discharge capacitance, the calculation of charging circuit design is much more complex. The voltage difference between capacitor C0 and capacitor C1 or capacitor C2 and the size of current limiting inductance will affect the charging current. Moreover, the voltage difference between capacitor C0 and capacitor C1 or capacitor C2 will continue to decrease with the discharge process, and the decreasing speed is related to the capacity of C0. In addition, the charging time is limited to the period when the capacitor is not discharged and the charging current shall not exceed the rated range of the switch. Figure 3 shows the waveform of theoretical charging current. The circuit equation of the charging circuit is also shown in the figure.

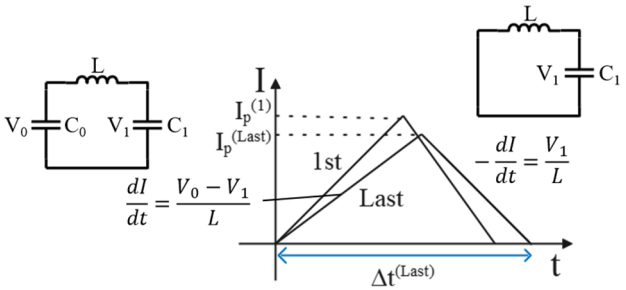

Figure 3: Theoretical charging current.

For the current waveform of the last discharge, the following equation can be listed. Since there is a compensation diode in the circuit, the amount of charge supplemented for each charge does not come entirely from C0. Assuming that half of it comes from C0, the relationship between the amount of charge compensated for each time q and the charging time and peak current is shown in the following formula.

$$\frac{1}{2} I_p^{(Last)} \Delta t^{(Last)} = q \tag{2}$$

The relationship between C0 voltage V0 and C1 or C2 voltage V1 and charging time, peak current and inductance L is shown in the following formula.

$$\frac{LI_p^{(Last)}}{V_0^{(Last)} - V_1} + \frac{LI_p^{(Last)}}{V_1} = \Delta t^{(Last)} \tag{3}$$

Similarly, for the current waveform of the first charge, the following relationship can be listed.

$$\frac{LI_p^{(1st)}}{V_0^{(1st)} - V_1} + \frac{LI_p^{(1st)}}{V_1} = \Delta t^{(1st)} = \frac{2q}{I_p^{(1st)}} \tag{4}$$

Where L is the inductance, is the peak current during the first charging, is the voltage at C0 at the beginning of the first charging, V1 is the voltage of C1 or C2, and is the

total time of the first charging process. The relationship between and is shown in the following formula.

$$V_0^{(1st)} = V_0^{(Last)} + \frac{Q}{2C_0} \quad (5)$$

Where Q is the amount of all charges consumed by discharge on the load, and C0 is the size of capacitor C0. Through the relationship of the above formula, the relationship between the voltage difference between C0 and capacitor C1 or capacitor C2, the inductance, the amount of charge consumed by each discharge and all charges consumed by discharge on the load can be obtained when the charging time is limited to the period when the capacitor is not discharged and the peak current does not exceed the rated current of the switch. The specific optimal parameter selection should judge which parameter has high priority according to the actual situation, and even decide with the help of a large number of calculations by computer.

SIMULATION RESULTS OF TEST CIRCUIT

We designed a prototype pulsed power circuit with the goal of ripple ± 1%, pulse width of 500 μs and output current of 80 A when the switching frequency is determined to be 50 kHz. While completing the verification experiment, try to realize the commercial standard ripple size and sub era standard pulse width on the prototype circuit.

Considering the energy loss in the circuit, we temporarily selected the C0 size 220 μF method, the charging voltage 750 V, the load resistance 5 Ω and the inductance size 5.33 μH to make the prototype circuit.

Before the experiment, the feasibility of the proposed circuit is analyzed by simulation. For the selection of simulation software, lt spice software is selected for circuit simulation. Figure 4 shows the circuit diagram used for simulation. Considering the large output current and serious overvoltage caused by excessive filter capacitor, a filter inductance of 5 μH and a filter capacitor of 10 nF are selected to further reduce the ripple.

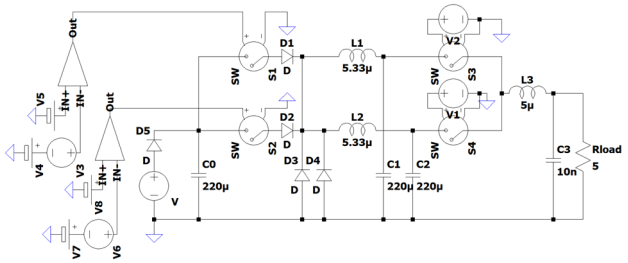

Figure 4: Circuit diagram for simulation.

Figure 5 and 6 is the result of the simulated output voltage waveform. As shown in the figure, the ripple of the output voltage waveform in the simulation is slightly less than 1%, which is consistent with the result of about 1% theoretical ripple in the theoretical calculation in the circuit design stage. Since the charging speed is not carefully adjusted, the voltage waveform is not very smooth.

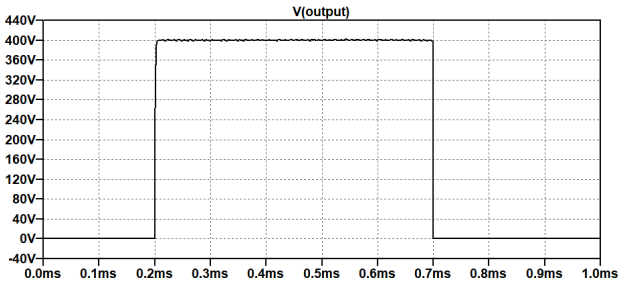

Figure 5: Output voltage waveform of simulation.

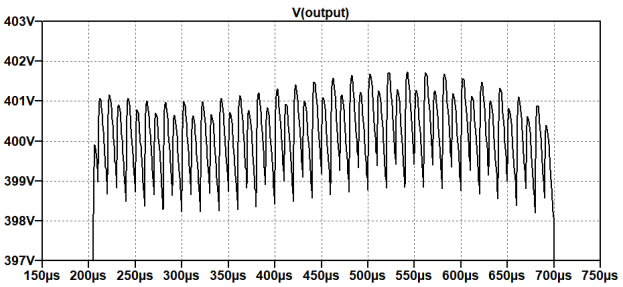

Figure 6: Amplified Output voltage waveform of simulation.

Figures 7, 8, 9 and 10 respectively show the voltage change of C1, the corresponding charging current waveform, the switch signal and the voltage change of C0, in a charging and discharging cycle. From the figure, the working condition of the capacitor is consistent with the idea put forward in the circuit conception stage. After one discharge, capacitor C1 is pulse charged through C0 and restored to the voltage before discharge.

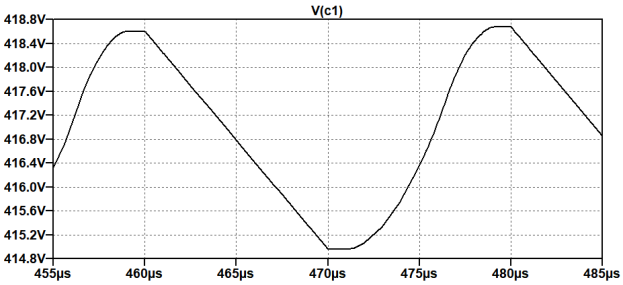

Figure 7: Voltage change of C1 of simulation.

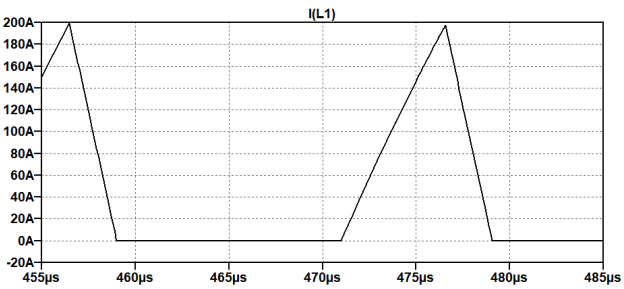

Figure 8: Charging current of simulation.

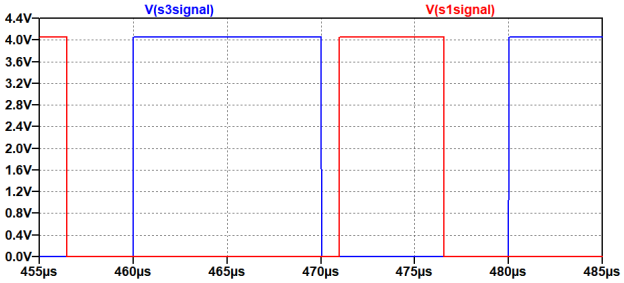

Figure 9: Switch signal of S3 and S1of simulation.

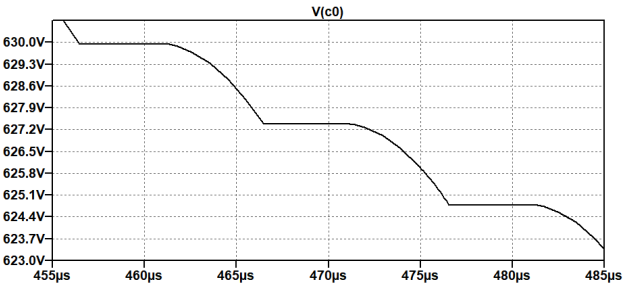

Figure 10: Voltage change of C0 of simulation.

TYPICAL EXPERIMENTAL RESULTS OF PROTOTYPE CIRCUIT

Typical output of the test circuit

The typical output of the test circuit is shown in Fig. 11 and 12. As shown in Fig. 11, the shape of the output voltage waveform of the trial circuit is basically consistent with the simulation results. It has the characteristics of fast rising speed and falling speed of long pulse power generator.

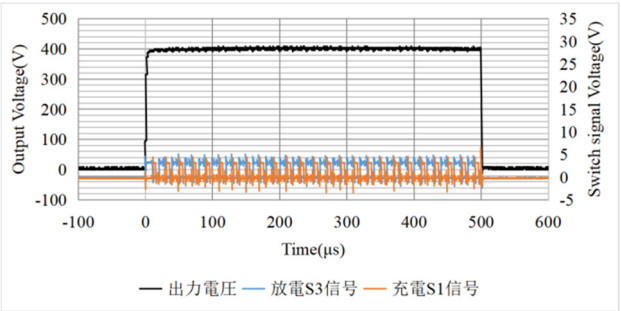

Figure 11: Typical output voltage waveform of test circuit.

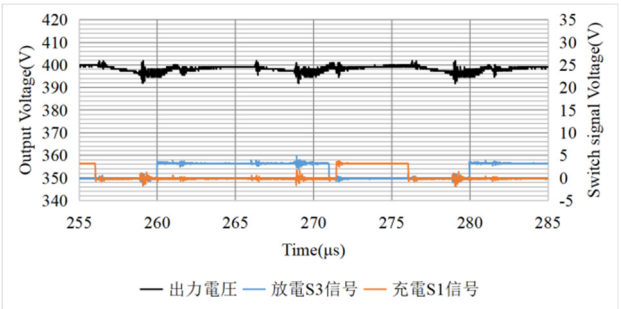

Figure 12: Amplified typical output voltage waveform of test circuit.

As shown in Fig. 12, the ripple of the waveform is about 1.5%, but some places have large noise due to the influence of electromagnetic coupling, which may act on the probe or directly on the discharge circuit. It has also been tried to use C1 and C2 with larger capacity to reduce the ripple size, but even if the capacity is doubled, the effect on ripple reduction is still small. As just mentioned, the reason why the ripple can not reach the level of the simulation of the circuit is mainly due to the influence of electromagnetic coupling and capacitor discharge speed. Simply increasing the capacity can not solve the above problems, so the trial circuit encountered difficulties in the experiment of further reducing ripple.

Although the problem of capacitor discharge speed is not so easy to solve without greatly increasing the volume, the problem of electromagnetic coupling can be expected to be solved. Secondly, because the shape of the output waveform is periodic and similar to sinusoidal waveform, the ripple can be reduced by phase control when forming a multistage circuit. If successful, this will be expected to achieve a ripple size of ± 0.5%.

Efficiency of test circuit

By measuring the waveform of the output current and the waveform of the capacitor C0, then integrating the charging current and calculating the change of the energy stored on C0 through the change of C0 voltage before and after the whole discharge process, and finally their ratio is the efficiency of the test circuit. Figures 13 and 14 show the waveform of output current and the waveform of C0 voltage change respectively. The final calculated circuit efficiency is about 72.8%. The energy loss of the circuit is mainly composed of the loss caused by switching and the resistance of the conductor.

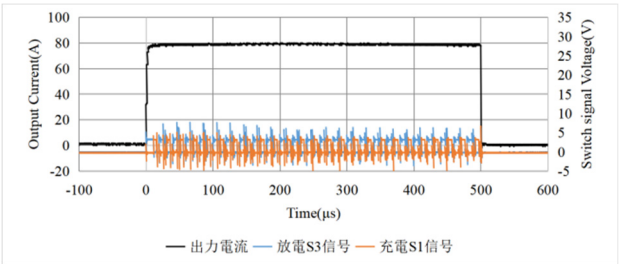

Figure 13: Typical output current waveform of test circuit.

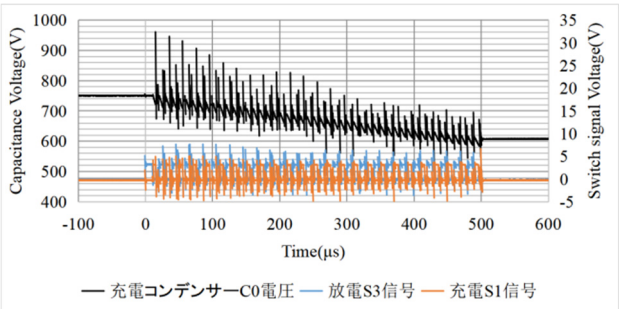

Figure 14: Typical output voltage waveform of test circuit.

CONCLUSION

In this study, a new pulse power circuit for realizing long pulse and low ripple is proposed and studied. Through theoretical calculation, software simulation, making test circuit and experiments, the following conclusions are obtained.

Firstly, by discharging the two capacitors alternately and then charging them during the period when they are not discharged, the drop of output voltage generated in long pulse capacitor discharge can be effectively suppressed.

Secondly, in the verification experiment, when the switching frequency is 50 kHz, the output with current of 80 A, pulse width of 0.5 ms and ripple of about 1.5% is realized.

Finally, the efficiency of the trial circuit was measured to be about 73%.

Although the circuit still has some difficulties in further reducing the ripple, it can be expected to obtain a more practical ripple output by improving the magnetic field shielding and phase control between multiple units. At the same time, the voltage drop compensation of long pulse is realized. Such long pulse low ripple voltage is likely to play a role in the development of accelerator in the future, so the further research of this circuit is also meaningful.

ACKNOWLEDGEMENTS

I would like to express my gratitude to all those who helped me during the writing of this thesis.

My deepest gratitude goes first and foremost to Professor Weihua Jiang, my supervisor, for his constant encouragement and guidance. He has walked me through all the stages of the writing of this thesis. Without his consistent and illuminating instruction, this thesis could not have reached its present form.

Secondly, I would like to express my deep gratitude to assistant prof. Taichi Sugai. Thanks to him for guiding my experiments and guiding the direction of the experiments.

I would also like to acknowledge my indebtedness to the senior Zhuang Longyu and many others who have contributed their time, thoughts, skills and encouragement to my study.

At the same time, I also want to thank to Associate Professor Sasaki Toru and Associate Professor Kikuchi Takashi for their helpful advice for my research.

Finally, I am indebted to my parents for their continuous support and encouragement.

REFERENCES

[1] C. Burkhart, A.Benwell, T.Beukers, M.Kemp, R.Larsen, M.Nguyen, J.Olsen, T.Tang, “ILC MARX MODULATPR DEVELOPMENT PROGRAM STATUS”, Pulsed Power Conference, pp. 807 810 (2009).

[2] T.Tang, C.Burkhart, M.Nguyen, “A VERNIER REGULATOR FOR ILC MARX DROOP COMPENSATION”, Pulsed Power Conference, pp. 1402 1405 (2009).

[3] Dr. Floyd Arntz, Dr. Marcel Gaudreau, Kevin Ostlund, Michael Kempkes, Dr. Jeffery Casey, “New Concepts for Puled Power Modulators: Implementing a High Voltage Solid-State Marx Modulator”, Vacuum Electronics Conference, pp.427 428 (2012).

[4] ILC Technical Design Report Volume 3 – Accelerator, 2013; `http://www.linearcollider.org/ILC/Publications/Technical-Design-Report`.