PERFORMANCE TEST AND INITIAL APPLICATION OF WHITE RABBIT SYSTEM AT SuperKEKB

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Abstract

The basic performance of the White Rabbit system is studied at KEK. The precision in the timestamp synchronization and the timing-trigger delivery is measured with the direct connection of two White Rabbit modules. The long-term stability of the timestamp synchronization is measured with the one master and two slave nodes configuration. The jitter of the PPS signals from two slave modules is 63.46 ps and stable for more than one week. This stable synchronization is realized by automatically measuring and calibrating the cable delay in every second. The initial application to the SuperKEKB operation is carried out in the 2020 spring run. The latency of the Abort Trigger System is measured with the common timestamp of the White Rabbit system. We configure the White Rabbit system for synchronizing its common timestamp with that of the Event Timing System. The common timestamp will be an important technology in the future SuperKEKB operation.

INTRODUCTION

The timing system is one of the most important components in particle accelerators. Its roles in the accelerator operations are the delivery of the timing-trigger, the RF clock, and the revolution signals.

The timing system consists of the timing devices that are installed along the beamline and the dedicated optical network that connects the individual timing devices. There are two major trends in the timing system in modern accelerators. One is Event Timing System (EVT) [1] and the other is White Rabbit (WR) [2]. In those systems, the timing device consists of the FPGA circuit and the SFP for the network interface. The operation clocks of the individual timing devices are precisely synchronized. It realizes the accurate delivery of the timing-triggers.

Recently, the advanced and sophisticated operation of accelerators is realized with the timing system. It is the fast and synchronized control of the remote hardware components via the timing system network. For example, the injector linac at KEK [3] carries out the pulse-to-pulse modulation of the beamline hardware in 50 Hz [4]. The distributed data acquisition system (DAQ) is planed at some institutes [5].

KEK considers the application of the WR system to develop the distributed DAQ at SuperKEKB [6].

In this report, we introduce the results of the basic performance tests of the WR system that are carried out at KEK. Then, the initial (and tentative) application to the SuperKEKB control system is discussed.

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WHITE RABBIT

The key technology of the WR system is the common timestamp in all remote devices. The timestamp of the WR device is determined from the FPGA clock which is synchronized with those of all other WR devices via the PTP (IEEE1588 standard) based network protocol.

The timing-trigger system can be configured with this common timestamp. The thermal drift of the cable delay is continuously calibrated so that the performance is stabilized during the long-term accelerator operation.

The WR system is developed in the open hardware project which is organized by CERN. It is the expanded concept of the open-source software and releases all information that is necessary to develop the hardware. There are several commercial suppliers that can provide the master device of the WR system. It enables the continuous and massive provision of the hardware. It is a strong advantage for large-scale and long-term projects like the SuperKEKB and future colliders.

PERFORMANCE TEST AT KEK

The basic performance is studied with the test bench which consists of the small amount of the WR modules. We utilize the two SPEC (Simple PCIexpress Carrier) boards [7] into which the FMC-DIO card [8] is inserted.

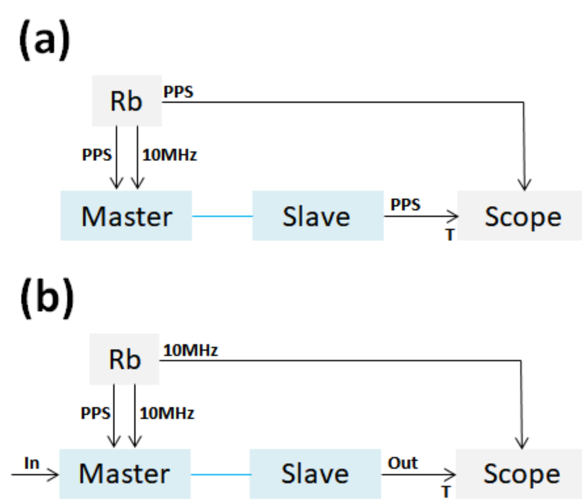

Figure 1: Setup of the precision measurement for the PPS signal (a) and the transferred timing-trigger (b): both "Master" and "Slave" are the SPEC board that is inserted into the PC.

Timing Trigger Transfer

Two kinds of performance tests in the timing-trigger transfer are carried out. One is the PPS (Pulse Per Second) signals comparison which can confirm the synchronization of the timestamps. The other is the measurement of the timing precision in the timing-trigger delivery. Their setups are shown in Figure 1. In both cases, the "Master" and "Slave" modules are configured with the SPEC boards and are directly connected. The PPS and 10 MHz clock signals from the Rb clock are provided to the master node. These setups refer to the instruction of the starting kit [9].

Figure 2 shows the results of the measurements by the oscilloscope, DPO7254. The upper figure shows the jitter of the PPS signals. It represents the precision of the timestamp synchronization and to be 131.8 ps. The lower figure shows the jitter of the timing-trigger which is transferred from the master to the slave modules. It is measured to be 137.5 ps. It is reasonable that the precision of the timing-trigger transfer is consistent with that of the timestamp synchronization[1].

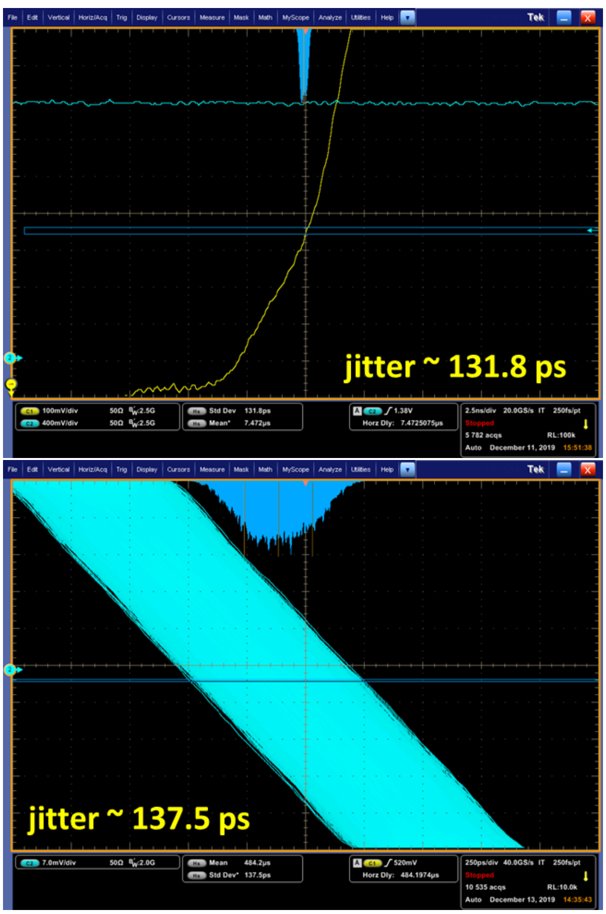

Figure 2: Results of the performance tests in the timing-trigger transfer: the resultant jitters of the PPS signals (up) and the transferred timing-trigger (down) are measured with the oscilloscope.

[1] Note, the precision becomes one order better in case of the RF clock delivery. Sometimes it makes confusion. However, it is the different result comes from the different system [10, 11].

Cable Delay Compensation

There is a cable delay when the signal is transferred via the optical cable. Its magnitude is typically 1 ns in the 20 cm cable. The WR system has the function to measure the cable delay for all connections under its network. Then, they are compensated when the common timestamp is established. The measurement of the cable delay and the replacement of the calibration factor for the common timestamp are implemented in every second.

Figure 3 shows the picture and the schematic view of the setup that we develop for the performance test of cable delay compensation. In this case, we put the WR switch [12] as the master module. Two SPEC boards are configured under this WR switch as the slave nodes.

Two SPEC modules are inserted into the adjoining PCs. However, the optical cable lengths from the master module are quite different. One is only 1 m and the other is about 8 km. The later connection is prepared with the optical cables between the central control building (CCB) and the D2 sub-control building of SuperKEKB. It is realized with the two round-trips connection between two buildings.

The time chart of the calibration factor for the 8 km-cable delay is shown in Figure 4. The data are plotted from February 6th, 9:10 am to February 13th, 9:25 am in 2020. The calibration factor is obviously correlated with the temperature at the KEK Tsukuba campus. Therefore, it is regarded that the timing drift of the cable delay caused by the thermal expansion of the cable length is compensated.

Figure 5 shows the jitter of the PPS signals from the two slave nodes. Also, this data are accumulated from February 6th, 9:10 am to February 13th, 9:25 am in 2020. The precision of the timestamp synchronization in this setup is excellent and to be 63.46 ps. And its long-term stability is also confirmed. The calibration system of the cable delay plays quite an important role since the cable delay is drifted about 5-10 ns in that period.

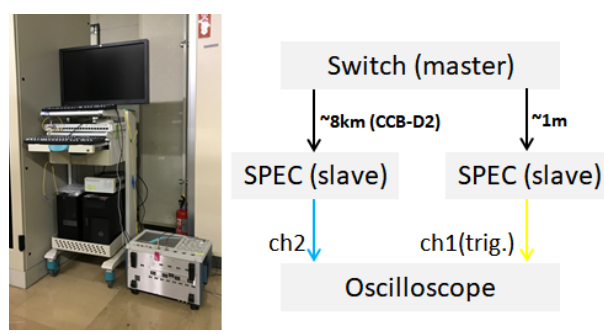

Figure 3: Setup of the performance test of the cable delay compensation: picture (left) and schematic view (right) of the setup is shown. Two slave nodes are connected with the master modules (WR switch) with the optical cables of 1 m and 8 km. The PPS signals from two slave nodes are measured with the oscilloscope.

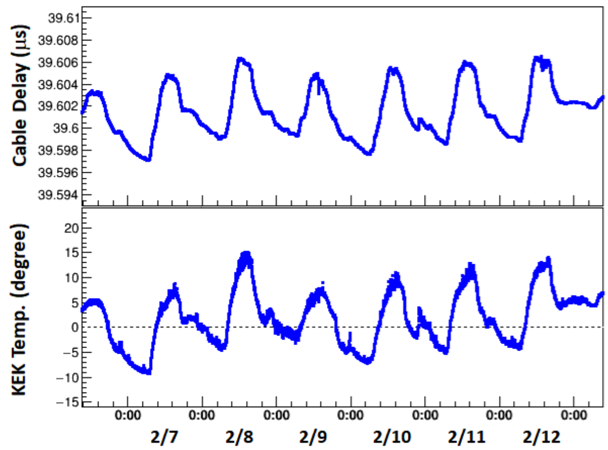

Figure 4: Time chart of the calibration factor for the 8 km-cable delay: the calibration factor is plotted in every second (up). The temperature at the KEK Tsukuba campus in the same period is plotted together (down).

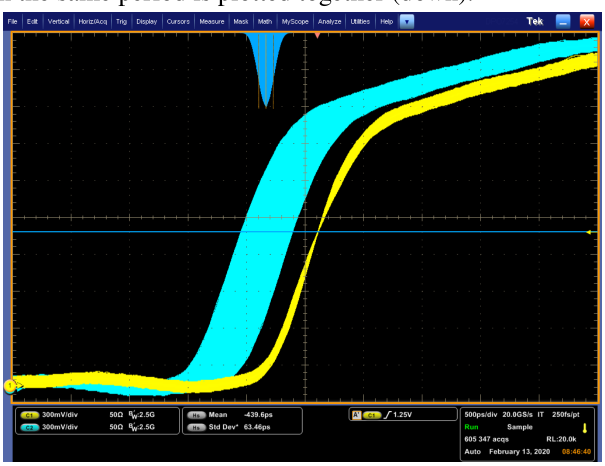

Figure 5: Comparison of the two PPS signals: the timing relation of the PPS signals from two slave nodes in Figure 3 is measured with the oscilloscope. The data are accumulated from February 6th, 9:10 am to February 13th, 9:25 am in 2020.

INITIAL APPLICATION AT SUPERKEKB

The initial application at SuperKEKB is realized in the 2020 spring run. The following two things are carried out in the accelerator operation.

Abort Response Measurement

The latency of the Abort Trigger System [13] is studied with the common timestamp of the WR system. The Abort Trigger System collects the abort request signals from the beamline hardware and launches the trigger to the abort kicker magnet. Therefore the abort response time depends on the latency of the Abort Trigger System.

The WR slave node configured with the SPEC board and the FMC-DIO card can record the timestamp when it receives the signal. The timestamp data recorded at different slave nodes can be compared thanks to the timestamp synchronization.

The latency of the Abort Trigger System is measured for both the positron and electron rings with the setup shown in Figure 6. The latency is measured with the WR system when the abort is requested from the hardware at the interaction point.

One slave node is placed at the D2 sub-control building. This node receives the reference signal when the Abort Trigger module receives the abort request signal from the hardware at the interaction point. The slave nodes should be placed in both the D7 and D8 buildings since the abort kicker triggers for the positron and electron rings are delivered there. However, we have only one remaining slave module. So the other slave node is placed at the CCB and it receives two kinds of abort kicker triggers. One abort kicker trigger is directly input into the slave node while the other is input after a round-trip to the D7 or D8 buildings. The cable delay from the CCB to D7 or D8 can be evaluated by comparing the timing of these two abort kicker triggers.

The latency of the Abort Trigger System, ΔT_{abt}, can be determined from the timestamps recorded on two WR slave nodes with the following formula:

$$\Delta T_{\mathrm{abt}} = (T_2 + T_3)/2 - T_1,$$

where T_1 is the timestamp when the D2 node receives the reference signal of the abort request. T_2 and T_3 are the timestamps when the CCB node receives the two kinds of the abort kicker triggers. In addition to the abort kicker triggers, the revolution signal is input at the CCB node and its timestamp, T_4, is recorded.

Figure 7 is the result of the latency measurement. The data are taken with the real abort events that occurred from March 20th to March 23rd in 2020. The clear correlation between ΔT_{abt} and the revolution timing, $\Delta T_{\mathrm{rev}} = T_4 - T_1$, is observed in both the positron and electron rings. This correlation is reasonable. SuperKEKB makes the RF bucket region where the beam-bunch is not stored (abort-gap). Then the stored beam is thrown by synchronizing the rising time of the abort-kicker pulse to this abort-gap. The result exactly shows the trend in the two abort-gaps operation[2]. The minimum latency in this measurement is 11.13 µs and 12.18 µs for the positron and electron rings, respectively. The small difference of the latency comes from the cable delay from CCB to D7 or D8.

Synchronization with Event Timing System

The WR system is installed at SuperKEKB by synchronizing its timestamp with that of the EVT. The timestamp of all EVT modules is synchronized with the PPS signal provided from the Rb clock. And it is also synchronized with the timestamp of the Abort Trigger System [14].

[2] SuperKEKB has been operated with the two abort-gaps filling pattern since the 2019 Autumn operation. It is to suppress the response time from the abort request to the beam abort.

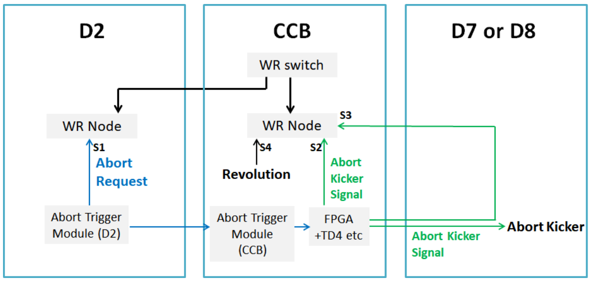

Figure 6: Schematic view of the latency measurement of the Abort Trigger System: two slave nodes are installed at the CCB and D2 buildings. The D2 node receives the reference signal when the Abort Trigger module receives a request from the hardware at the interaction point. The CCB node receives the revolution and the abort kicker signals. Two kinds of the abort kicker signals are input to consider the cable delay from the CCB to D7 or D8 buildings.

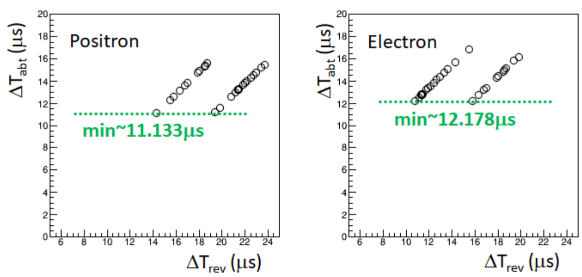

Figure 7: The 2-dimensional plot between ΔT_{abt} and ΔT_{rev}: the results for both positron (left) and electron (right) rings are plotted.

We configure the WR master module with the PPS and 10 MHz inputs from the same Rb clock. The synchronization of the common timestamps between the WR and EVT systems is realized with this configuration.

The quality of the timestamp synchronization is studied by comparing the PPS signals from the slave modules of the two systems. The timing difference and jitter are discussed in this comparison. The measurements are carried out in two places (the two sets of EVT and WR slave nodes). In both cases, the timing of the WR-PPS signal is measured by triggering the EVT-PPS signal. Figure 8 is the pictures of the measurement by the oscilloscope.

First of all, the jitter between two PPS signals comes from the difference in their FPGA clock rates. The WR system is operated with the FPGA clock of 125 MHz while the EVT is operated with that of 114.24 MHz. And they are not synchronized. In both measurements, the measured jitter becomes 8.75 ns in the full size. It is consistent with one EVT clock period.

The timing difference between two PPS signals is to be 4.19 μs and 4.44 μs. They are caused by the absence of the cable delay compensation in the EVT system. In other words, we measure the cable delay in the Event delivery by using the WR system.

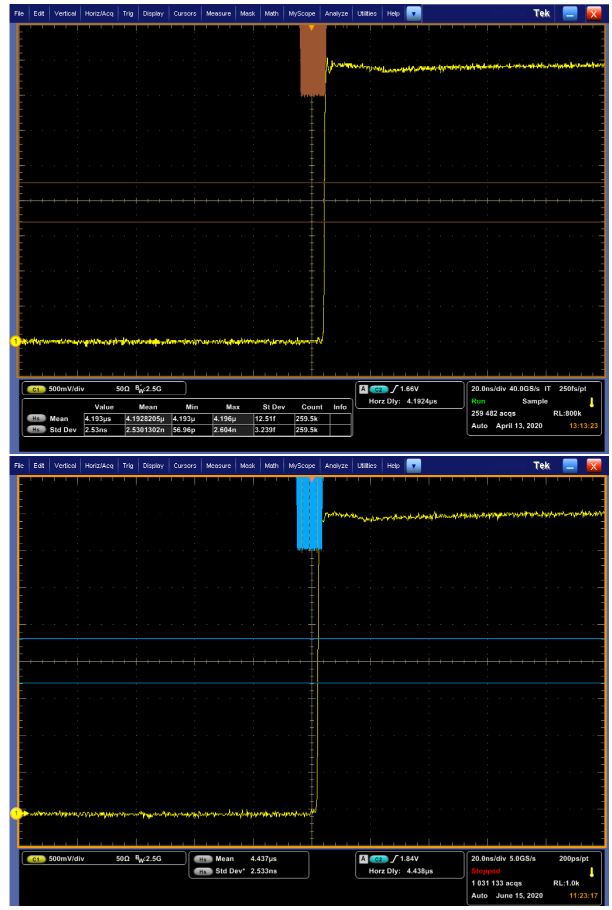

Figure 8: Comparison of the PPS signals between EVT and WR: two pictures show the results taken at two different places. In both cases, one division in the horizontal axis corresponds to 20 ns.

We must consider the above two information when we discuss the precision of the common timestamp between the WR and EVT systems. If we know and calibrate the cable delay between the EVT master and slave modules, the precision of the common timestamp comes from the jitter and to be 8.75 ns. However, this condition is optimistic since it is hard work to measure and calibrate the cable delay for all connections of the EVT modules.

We must regard the timing difference of the PPS signal as the precision of the common timestamp if we operate them without the understanding of the cable delay in the Event delivery. It is estimated to be, in maximum, ~15 μs when we consider the length of the optical cables that are put around the SuperKEKB beamline. This estimation should be considered as the precision of the common timestamp.

The common timestamp is the key tool for the error analysis in the accelerator operation. Besides, the distributed DAQ system at SuperKEKB is developing based on this common timestamp. Therefore, the application of the WR system can enhance their performances.

The initial application of the WR system reported in this section. However, it is a temporal system and the concrete design is on-going. It should include GPS for enhancing convenience. In any case, we plan to configure the common timestamp between the WR and EVT system. It will become a large advantage in the future SuperKEKB operation.

CONCLUSION

The basic performance of the WR system is tested at KEK. The precision of the timestamp synchronization is measured in the direct connection of two WR modules. It is consistent with the precision of the timing-trigger delivery in the same setup.

The long-term stability of the timestamp synchronization is confirmed. It is realized by compensating the timing drift caused by the thermal expansion of the optical cable. The WR system can compensate it by automatically measuring and calibrating the cable delay in every second for all optical connections.

The initial application to the SuperKEKB operation is carried out in the 2020 spring run. The latency of the Abort Trigger System is measured with the real beam-abort events at both positron and electron rings. The clear trend of two abort-gap operation is observed.

We establish the common timestamp between the WR and EVT systems by synchronizing the timestamp of the WR system with that of EVT. The precision of the common timestamp can be evaluated to be $\sim$15 µs. This comes from the lack of understanding of the cable delay in the Event delivery. If we measure and calibrate the cable delay for all Event module connections, the precision of the common timestamp becomes 8.75 ns that is the one clock period of the EVT operation.

The concrete design of the WR system application is on-going. It includes GPS. And in any case, the common timestamp between the WR and EVT system is established. It will become a large advantage in the future SuperKEKB operation.

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