Present Status of Digital Feedback and Feedforward Project Using Red Pitaya STEMlab

On behalf of the J-PARC Linac RF Group

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Outline

- ❖ Red Pitaya STEMlab board
- ❖ Prototype Red Pitaya Digital Feedback system
  - FPGA Design
- ❖ Measurements and Results
  - ADC and DAC output performances
  - IQ Modulator and Demodulator Errors
  - Amplitude and phase stability of the RF field
- ❖ Conclusion

Section 01

Red Pitaya STEMlab Board125-14

❖ A brief introduction to the Red Pitaya STEMlab

★ To build a new Digital Feedback (DFB) system with a Red Pitaya board featured by;

- ➡ High performance,
- ➡ Low cost,
- ➡ Reconfigurable instrumentation and open source
- ➡ Small size

★ To use for the RF cavities in Muon LINAC for muon g-2/EDM Experiment project at J-PARC and RFQ cavity in Turkey.

Main steps for the Red Pitaya DFB system

❖ Hardware

❖ Firmware

- Construction of HDL codes and FPGA design (Xilinx Software - Vivado)

❖ Software

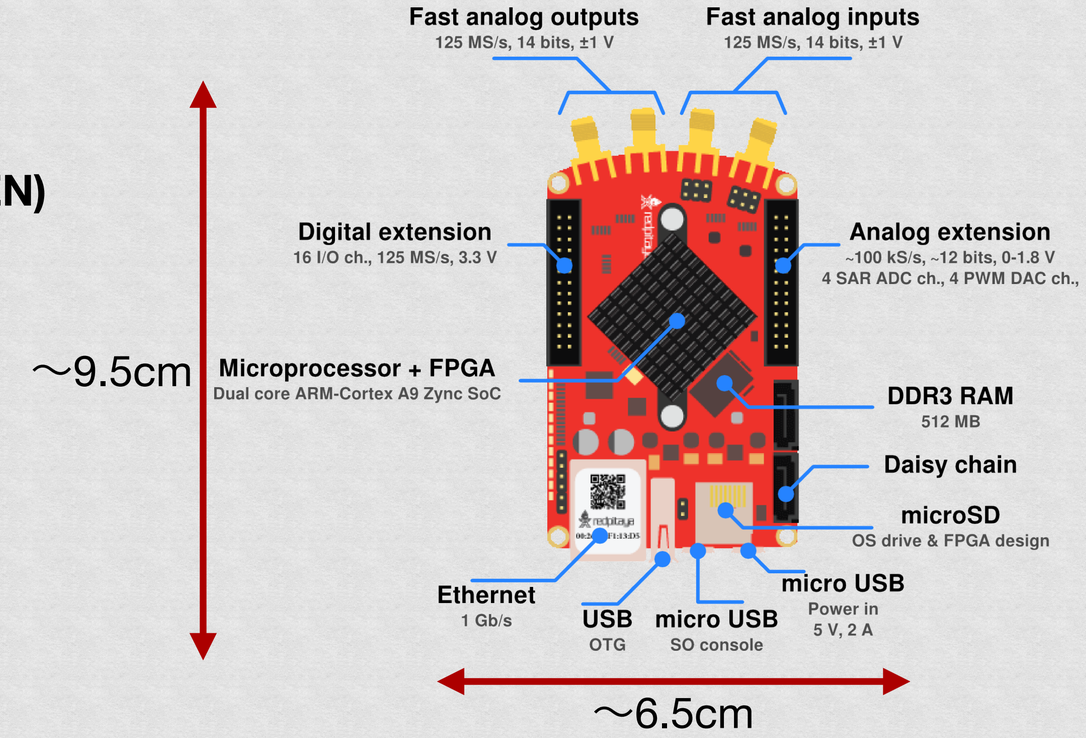
- EPICS Base; redpitaya-epics “driver” support. https://github.com/AustralianSynchrotron/redpitaya-epics
- MEMORY: A driver based on C language (RP DFB code)
- Creation of EPICS IOC
- Monitoring: Graphical User Interface (GUI) with CS-Studio

❖ Preliminary test and measurements

- ADC & DAC performance, IQ Mod./Demod. errors, amplitude and phase stability etc.

Basic:

- ❖ Red Pitaya STEMLab125 14
- ❖ High performance, small size, **low cost (~70k Japanese YEN)**
- ❖ Reconfigurable instrumentation and **open source**
- ❖ Processor: Dual core ARM Cortex A9
- ❖ FPGA: Xilinx Zynq 7010 System-On-Chip (SoC)

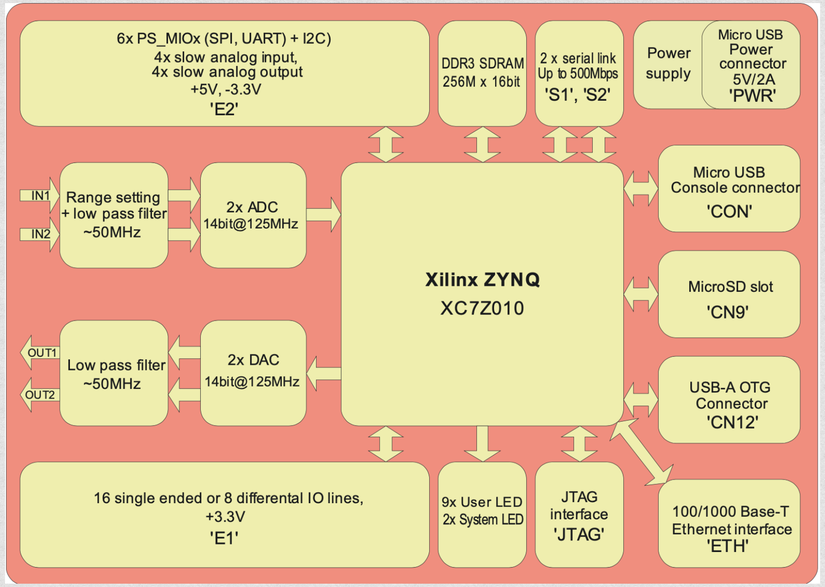


Extension connectors:

- ❖ Digital IOs:16ch (8 differential or 16 single-ended)
  - One of the DIOs is used as RF GATE

RF inputs/Outputs:

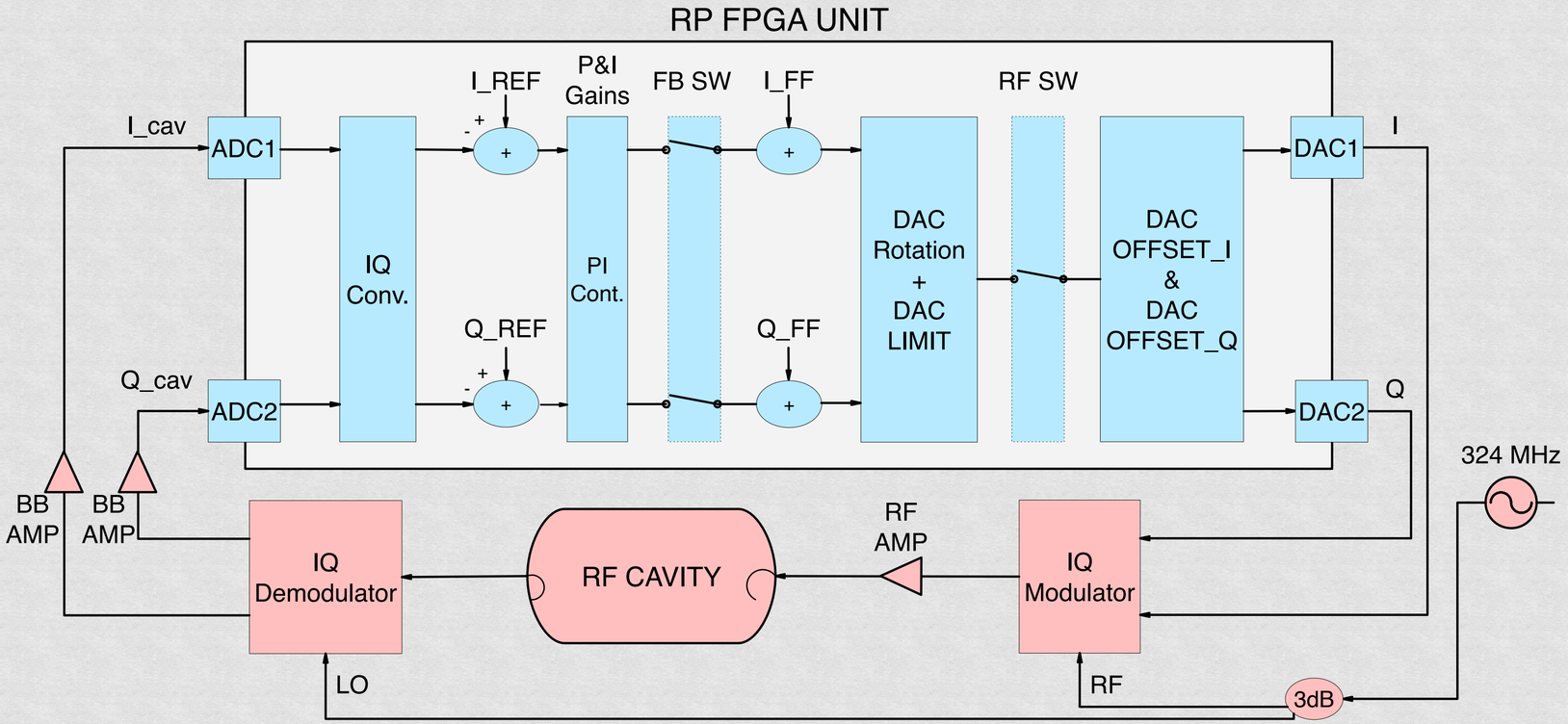
- ❖ Two 14bits ADC and DAC
  - Sample rate:125MS/s
  - Connector type: SMA
  - Two configurable voltage ranges: **±1 Volt** or ±20 Volt
  - Bandwidth: 50 MHz



Section 02

Prototype Red Pitaya DFB system

❖ Fundamental information about the whole system



All hardware is provided by J-PARC facility resources

HARDWARE List
Red Pitaya STEMlab 125-14 board https://www.redpitaya.com/f130/STEMlab-board
IQ Modulator (Passive)
IQ Demodulator (Passive)
RF Cavity
A Signal Generator (Agilent 8648B) https://www.keysight.com/ca/en/home.html
Baseband (BB) Amplifiers are used to amplify the Demod. output to work with ADC full scale home-built → built at J-PARC by project team.

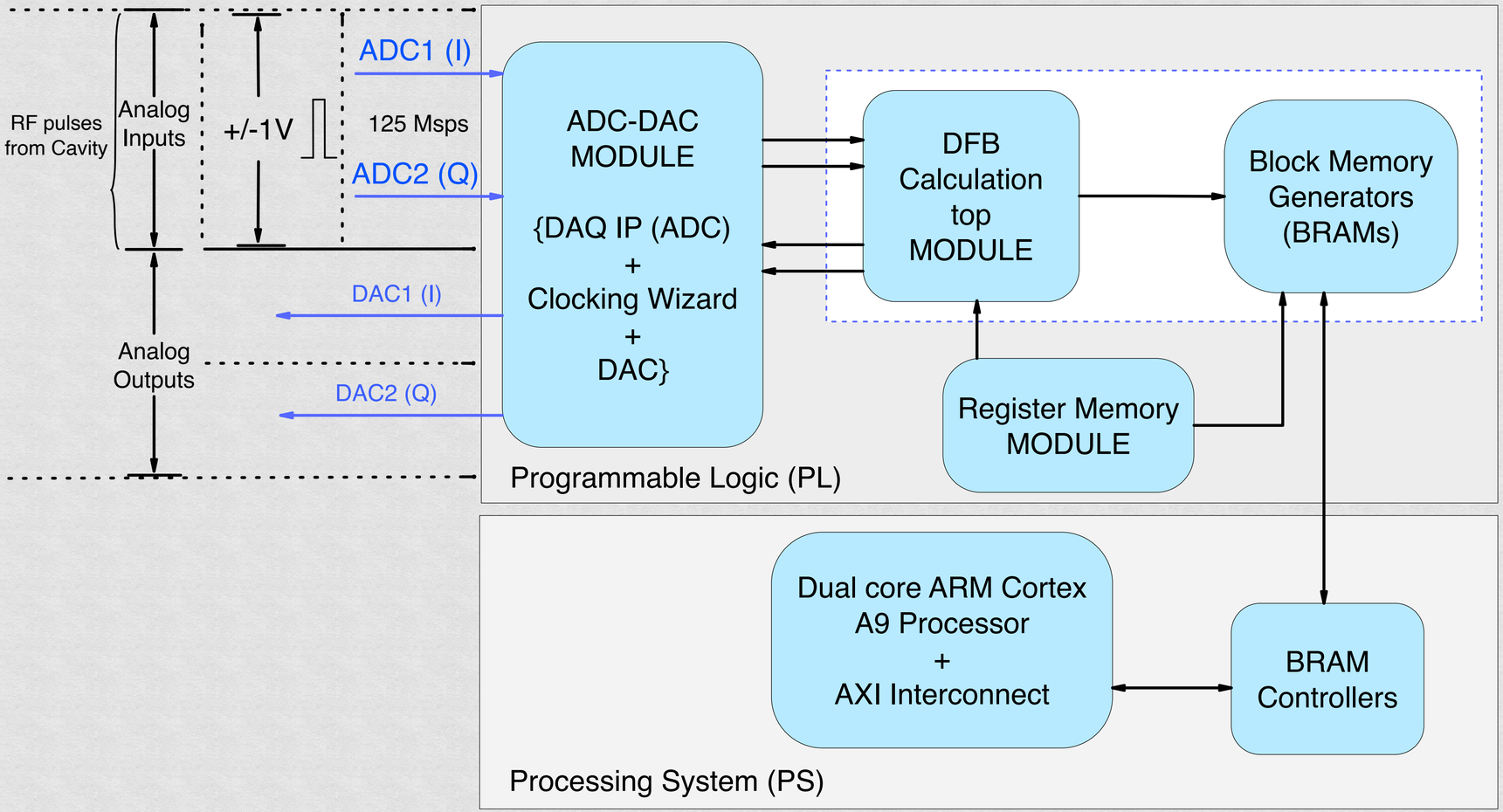
Features:

- Easy installation without synchronization using IQ Mod&Demod.
- ADC & DAC rotational functions with correction parameters for IQ Mod. and Demod.
- A PI feedback control
- Post-mortem use of data for ADC output waveforms to analyze
- Adjustable DAC outputs with Limit module

Section 02.1

FPGA Design

❖ Fundamental information about the FPGA design



- Design: Use of Vivado based on Intellectual Properties (IP) Core elements and User created custom IPs
- 16-bits sign extended ADC values

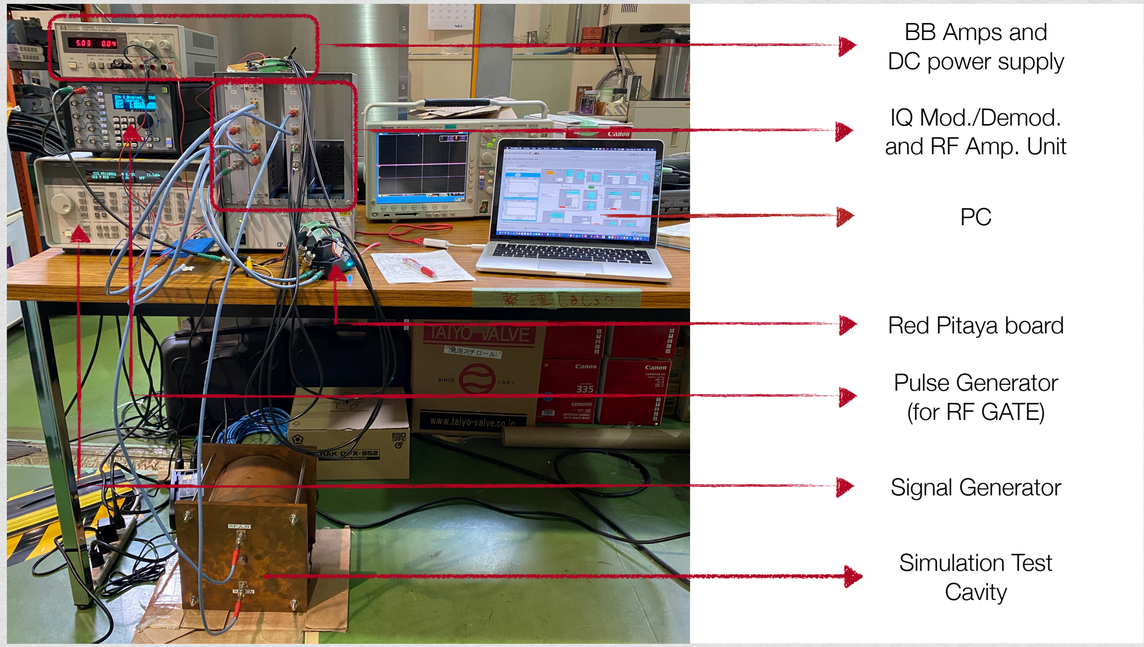
- Calculation top: Includes all RP DFB calculation IPs
- Register Memory: Used to help with updating record values for the EPICS IOC
- BRAMs: Writes ADC output values with a user-adjustable specific trigger rate
- Processing System + AXI Interconnect: Data transfer bus (Bus AXI) + Memory (RAM)

Section 03

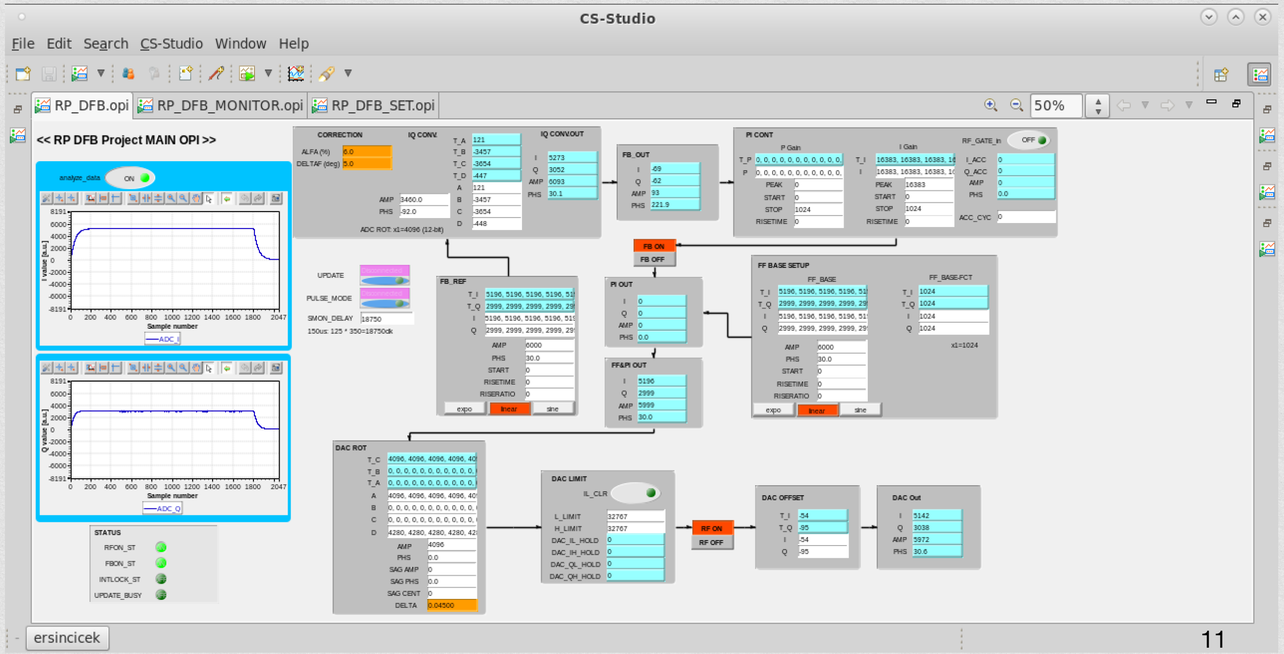
Measurements and Results

- Preliminary results

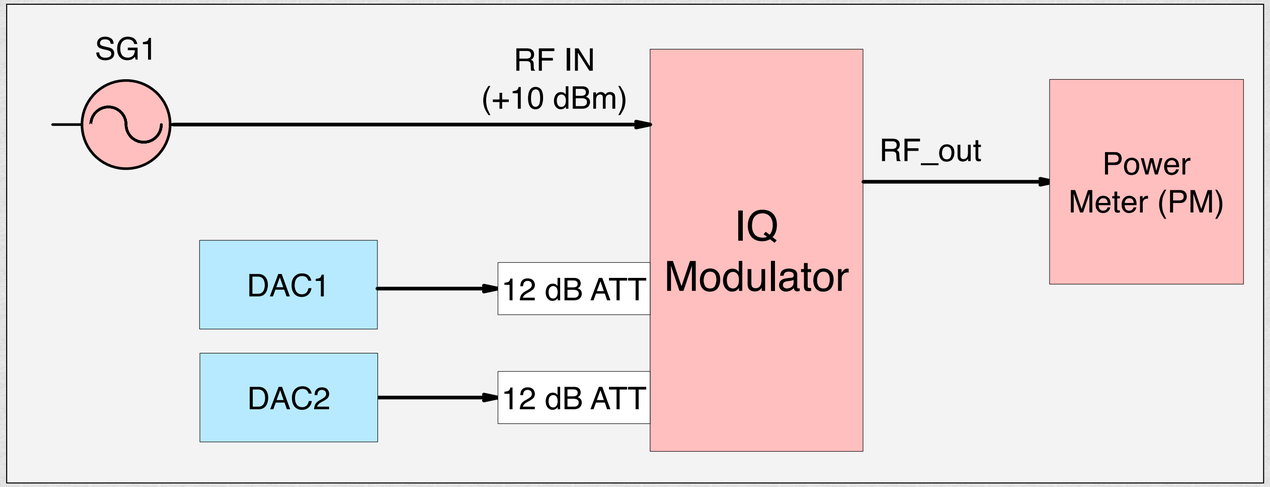
- Tests for the system are conducted on the ''simulation test cavity''.
- The performances of the hardware are investigated (ADC&DAC, IQ Mod.&Demod.)
- Amplitude and phase stability of the RF field is measured.



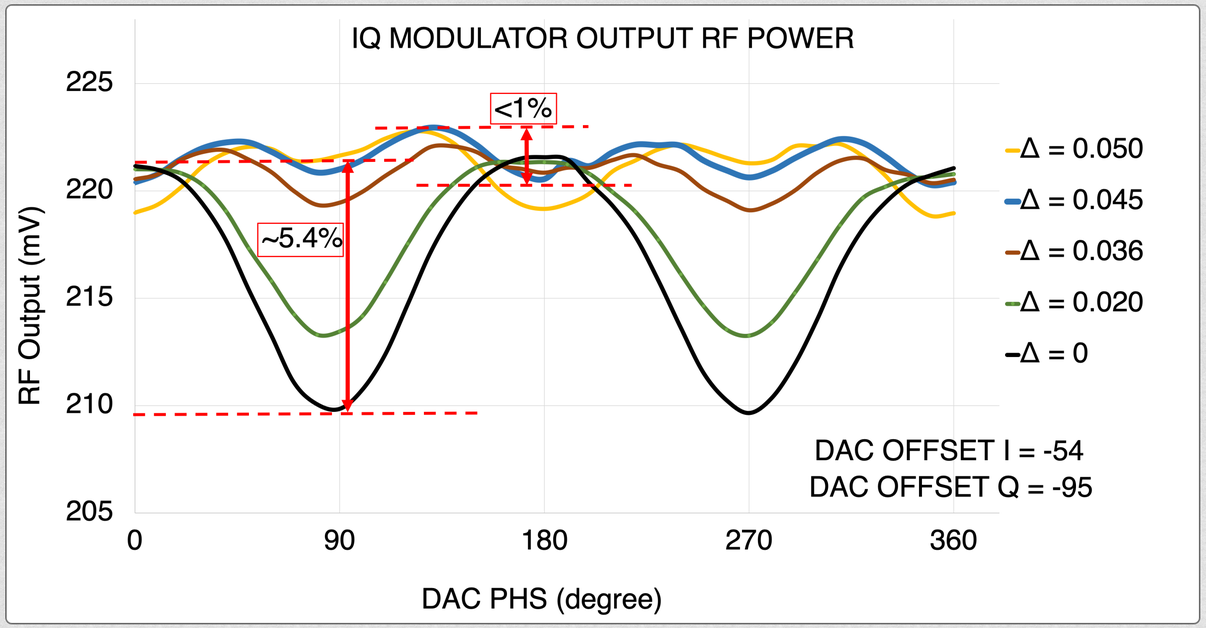
- The EPICS Base is cross-compiled.
- The EPICS IOC runs on the board itself with an executable file
- GUI with CS-Studio to access the EPICS PVs is used for monitoring and controlling the whole system.



IQ Modulator Errors

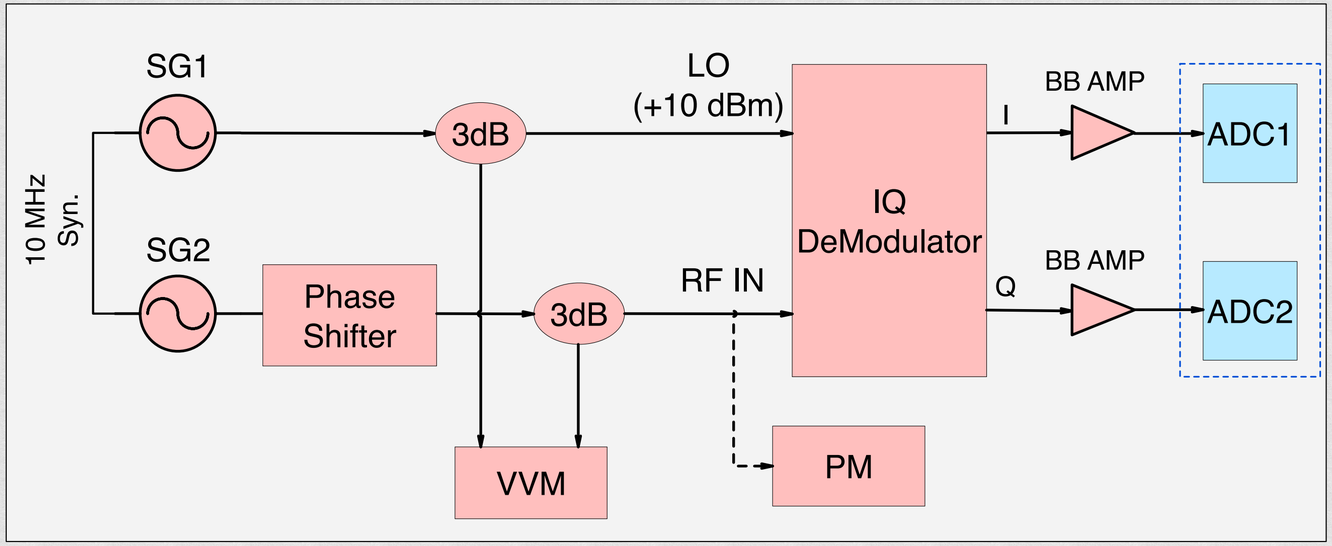


- Linearity error of IQ-Mod. output is measured by PM (Giga-tronics 8542C, https://go-asg.gigatronics.com).
- RF output is measured about 220 mV with several correction parameter (Δ)
- 12 dB ATTs are used to get the best performance in the Mod.
- The linearity error in the IQ Modulator output is about 5.4% (Δ=0)

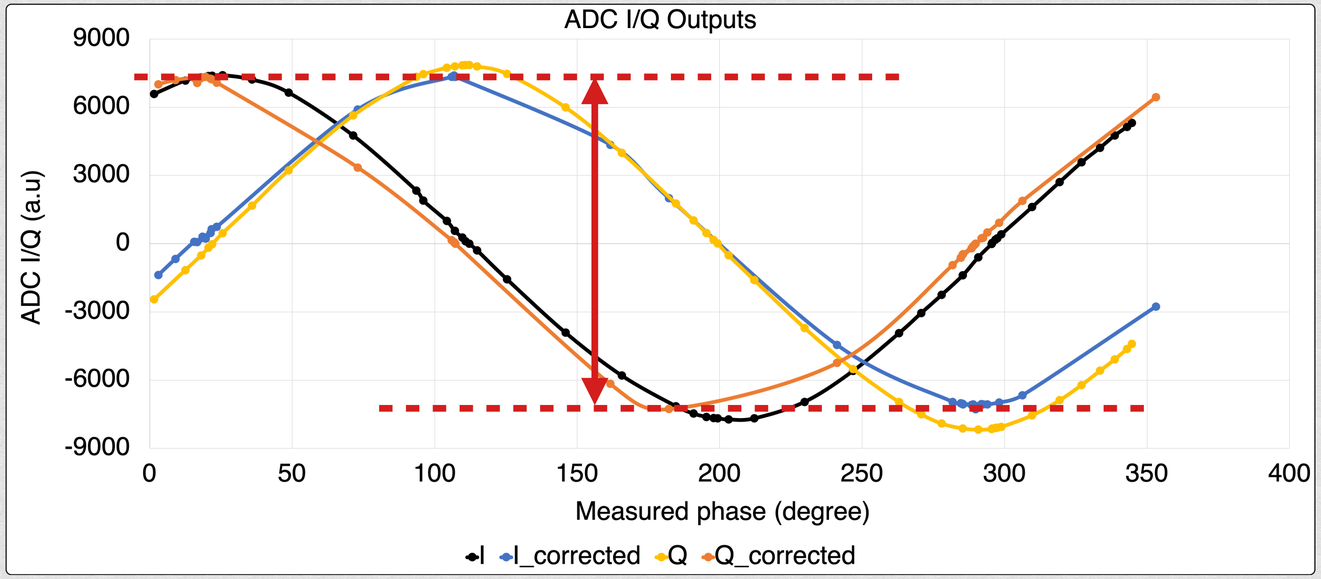


- IQ-Mod. output is corrected by the use of DAC rotational parameters with Δ.
- <1% error is achieved (Δ=0.045, **DAC AMP=7700**).
- Includes all errors in the setup such as ATTs.

IQ Demodulator Errors



- The errors at the IQ-Demod. output are measured by using ADC outputs and Vector Voltmeter (VVM) (Keysight N9913A, https://www.keysight.com/ca/en/home.html)
- Linearity error → 6%, Phase balance error → 5 degrees



- Output is corrected by the use of ADC rotational parameters and correction parameters, α and $\Delta\phi$.

After the correction

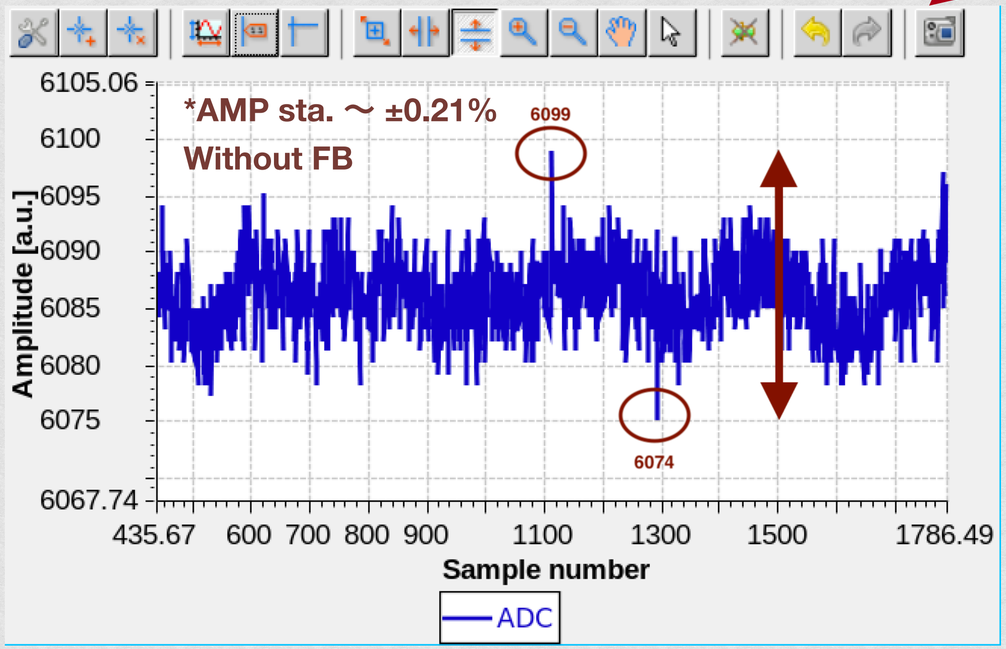
- For α=6% and$\Delta\phi$=5 degrees; **Linearity error → 0.08%, phase error → 0.45**

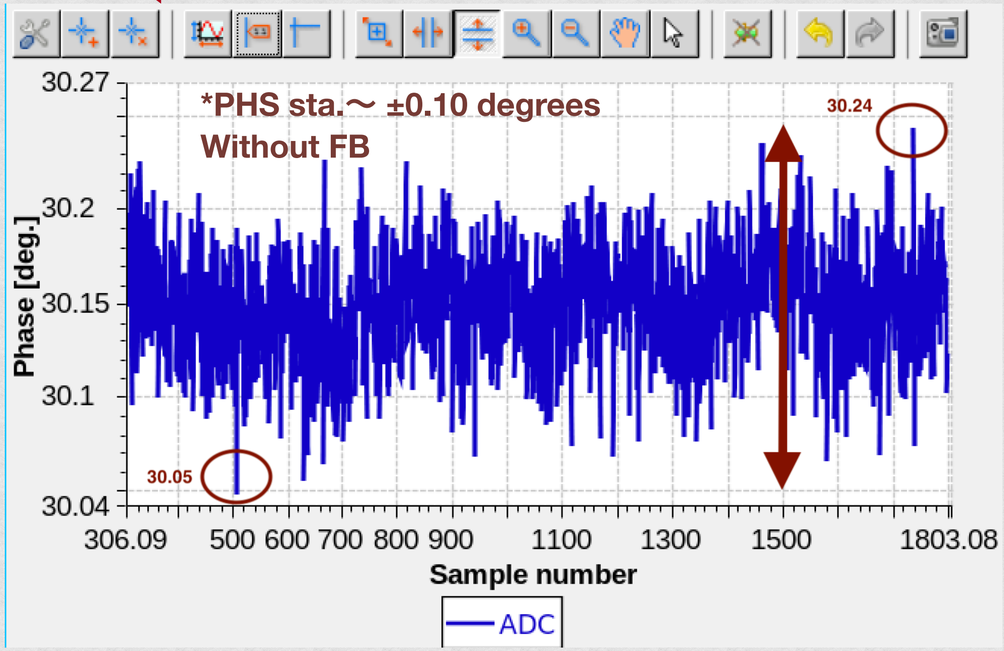
Summary of results

Hardware	Linearity Error [%]	Phase error [°]
DAC1	0.32	
DAC2	0.27	
ADC1	0.23	<2 (ADC)*
ADC2	0.08	
IQ Modulator	5.4 (<1)	
IQ Demodulator	~6 (0.08)	~5 (0.45)

{*} Linearity error of the ADC output phase (ADC is the sum of I and Q components)

- The system is tested by the use of ”Simulation Cavity”.
- Pulsed operation, RF signal 230 μs.
- The stability of RF field in the simulation cavity
- P gain is already satisfied, the study for I gain will be performed in the PI control.





Conclusion

- ✓ Hardware and software installation of the system has been successfully carried out.
- ✓ Preliminary tests are conducted on a simulation test cavity.
- ✓ The linearity error of less than 1% is achieved for IQ Modulator output power after correction.
- ✓ The linearity error of 0.08% and phase error of 0.45 degrees are achieved for IQ Demod. after correction.
- ✓ The error of the RF field is within ±1 degrees in phase and ±1% in amplitude is successfully required.
- ✓ The setup can be operated for pulsed operation and is effective for the RF pulses of <230 μs.
- ✓ Total cost is about 70k Japanese YEN which is one of key point of our system.

Future Plan

➡ The hardware in the system will be upgraded,

- IQ-Modulator (~13k JPY) and Demodulator (~16k JPY) with higher performance/less error.

➡ The setup will be used at:

- Linac section dedicated to the Muon acceleration for Muon g-2/EDM Experiment at J-PARC,
- And, it can be used in RFQ cavity in Turkey operating in pulsed mode with 100 μs RF pulses.

➡ The system will be upgraded to operate for 500 μs RF pulses. Hence;

- PI-Feedback will be tested in R&D of RFQ IV installed in Test Stand (TS) and Klystron TS in J-PARC

Thank you for your kind attention..

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ございました

References

[1] “Red Pitaya STEMlab 125-14’ https://www.redpitaya.com

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[6] “red-pitaya-notes”https://github.com/pavel-demin/red-pitaya-notes

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