RECENT PROGRESSES IN THE LLRF FPGA CONTROL SYSTEM OF THE J-PARC LINAC

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Abstract

The recent progresses in the LLRF FPGA control system of the J-PARC LINAC will be presented in this paper. Firstly, automatically switching the beam loading compensation in accordance with the different beam operation mode has been realized by the FPGA. Secondly, a chopped-beam compensation for the 972-MHz high-β section has also been performed by the FPGA. Finally, besides the mechanical tuning method of rf cavities, an input rf-frequency tuning has been carried out by the FPGA.

INTRODUCTION

The energy of the J-PARC proton LINAC will be upgraded from 181-MeV to 400-MeV, by adding a 972-MHz high-β section. For the RF systems of both the present 324-MHz low-β section and future 972-MHz high-β section, the RF amplitude and phase of the cavities are controlled by an FPGA-based digital feedback control system. The digital LLRF control system is installed in a compact PCI (cPCI), as shown in Fig.1. It consists of the CPU, IO, DSP with FPGA, Mixer & IQ modulator, and RF & CLK boards [1-4]. A very good stability of the accelerating fields has been successfully achieved about ±0.2% in amplitude and ±0.2 degree in phase, much better than the requirements of ±1% in amplitude and ±1 degree in phase. In the recent one year, a lot of progresses have been achieved in the LLRF FPGA control system for a more-convenient operation of the J-PARC LINAC with a high stability, especially for the 972-MHz high-β section of the J-PARC LINAC.

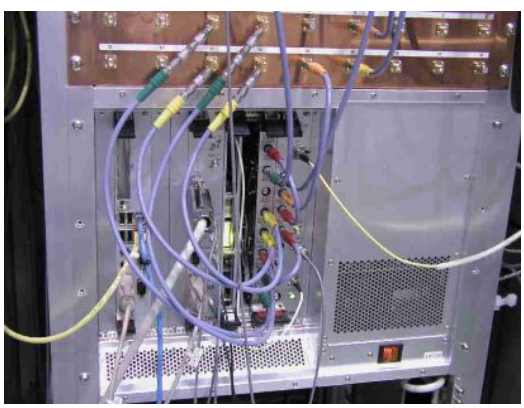


Fig. 1: Digital LLRF control system installed in a compact PCI.

AUTOMATICALLY SWITCHING THE BEAM LOADING COMPENSATION

Different beam operation modes, such as different beam current, are considered for the J-PRAC LINAC. The beam loading will be different from each other of operation modes. A control system with automatically switching the beam loading compensation is required, and it has been realized by the FPGA control program.

We add a mode-exchanging signal to the LLRF control system, which is called as FF_Beam_Mult gate with a different pulse width, corresponding to the different beam operation mode. The timing of the LLRF system is shown in Fig. 2. The pulse width of the FF_Beam_Mult could be from 1 μs to 50 μs. This signal is connected to the IO board of the cPCI and will be detected by the FPGA. Then in the FPGA control program, the different value of the feeding forward for the beam loading compensation (FF_beam) will be applied corresponding to the pulse width of the FF_Beam_Mult gate as shown in the Table I. Since the pulse width of the FF_Beam_Mult gate is detected before each pulse of FF_beam, switching the beam loading compensation will also be realized before each pulse, without any delay, even for one pulse. This function has been successfully tested in the present J-PARC LINAC. The application will be applied for both of the 324-MHz low-β section and 972-MHz high-β section of the J-PARC LINAC.

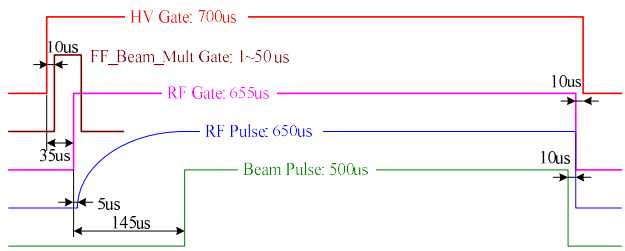


Fig. 2: Timing of the LLRF system.

Table I: Different value of FF_beam corresponding to the pulse width of FF_Beam_Mult gate.

Pulse width (us)	FF_beam
5 (04～06)	Amplitude_1 , Phase_1
10 (09～11)	Amplitude_2 , Phase_2
15 (14～16)	Amplitude_3 , Phase_3
20 (19～21)	Amplitude_4 , Phase_4
25 (24～26)	Amplitude_5 , Phase_5
Others	Amplitude_1 , Phase_1

CHOPPED-BEAM COMPENSATION

For the 972-MHz high-β section, the operation frequency is three times of that of the low-β section, and the decay time of the RF field becomes quite shorter. In this case, for a chopped-beam operation, a chopped-beam compensation is desired instead of a macro-pulse compensation. This function has also been performed by the FPGA control program.

In the chopped-beam operation, the beam will be modulated by a chopping signal as shown in Fig. 3. The frequency of chopping signal is about 1 MHz. We connect this chopping signal to the IO board of the cPCI control system. Then in the FPGA control program, the FF_beam is fed forward when the logical AND with inputs of the beam gate and chopping signal has the value 1. Also, in order to adjust the timing between the chopping signal and beam pulse, a delay is added to the chopping signal before the logical AND operation. This delay could be exactly adjusted in a clock of 48 MHz in the FPGA.

A test result for the chopped beam compensation is shown in Fig. 4 by using a cavity simulator [5]. A stability of the accelerating fields has been successfully achieved about ±0.4% in amplitude and ±0.3 degree in phase.

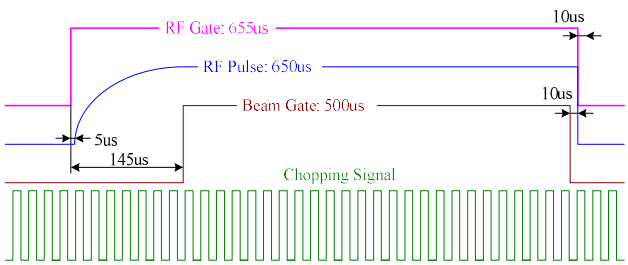


Fig. 3: Chopping signal and timing of the LLRF system.

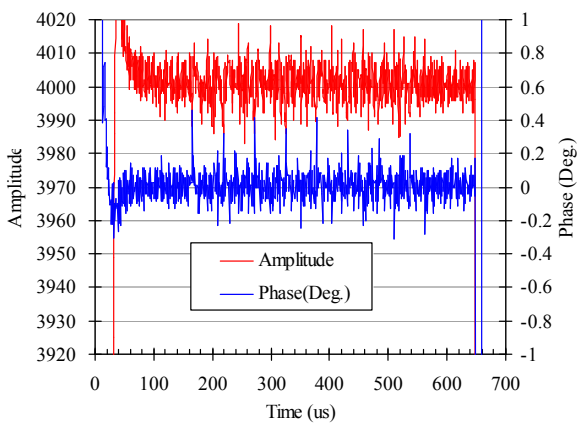


Fig. 4: Test result for the chopped beam compensation.

Now, two sets of FPGA programs, with chopping and without chopping, are prepared for the high-β and low-β sections, respectively. This will be unified to one FPGA program in the next coming moths by adding a control parameter in PLC touch panel.

INPUT RF-FREQUENCY TUNING

The mechanical tuning method is used for the present rf cavities of the 324-MHz low-β section. Besides, another method with input rf-frequency tuning has also been carried out by the FPGA.

The detuned frequency (Δω) of the rf cavities from the operation frequency will be detected from the cavity phase decay curve [6],

$$\Delta\omega = \frac{d\theta}{dt}.$$

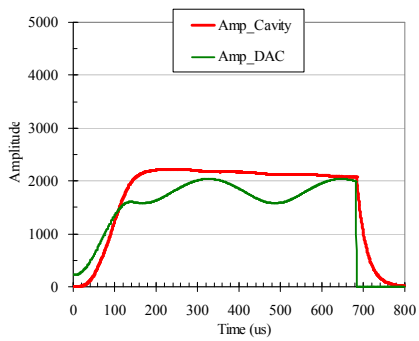
Then the input rf-frequency will be controlled by the FPGA to match the rf cavities. The input feeding forwards of I and Q to the IQ modulator are calculated in the FPGA as

$$FF\_I = FF\_base\_amp \times \cos(\Delta\omega \cdot t),$$

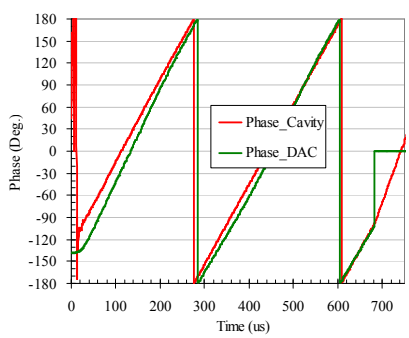
$$FF\_Q = FF\_base\_amp \times \sin(\Delta\omega \cdot t).$$

The experiment of the input rf-frequency tuning method has been successfully carried out at the DTL03 of the J-PARC LINAC. Fig. 5 shows an example of the RF waveforms of the cavity and DAC during the rf start-up at the DTL03. In the Fig. 5, 1a) and 1b) show that at middle of start-up, 2a) and 2b) at end of start-up, and 3a) and 3b) after FB ON, respectively.

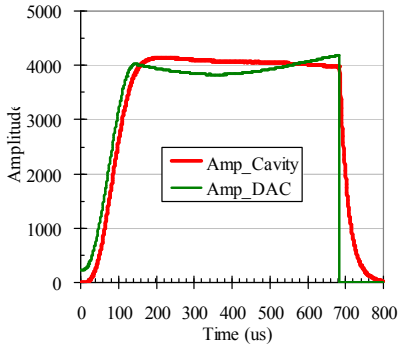
From the Fig. 5, during the whole process of rf start-up, the gradients of the phase slope in the driving rf pulse (before 685 μs) and in the field free decay (after 685 μs) are always almost same. That means that the input rf frequency is exactly matched to the cavity resonance frequency in the whole process of rf start-up. In the mean time, the gradient of the phase slope gradually become small due to the cavity warming. Finally the resonance frequency goes back to the operation frequency.



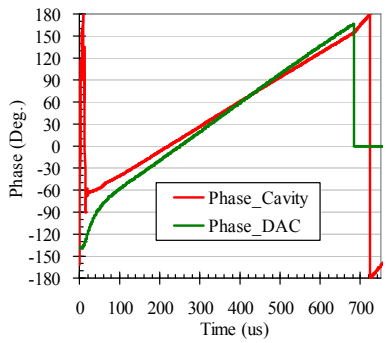
1a) amplitude at middle of start-up.



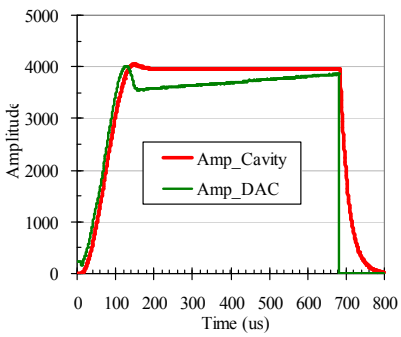
1b) phase at middle of start-up.



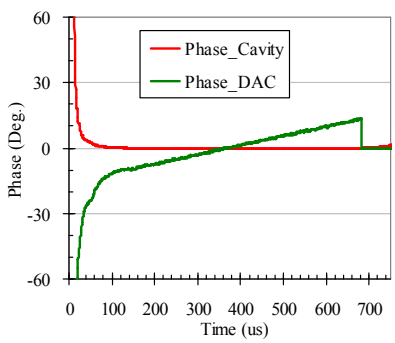
2a) amplitude at end of start-up.



2b) phase at end of start-up.



3a) amplitude after FB ON.



3b) phase after FB ON.

Fig. 5: RF waveforms of the cavity and DAC during the rf start-up at the DTL03.

On the other hand, for each step during the rf start-up in the Fig. 5, the amplitude of cavity is almost a constant, while that of the DAC varies with the time. In our system, an IQ offset has been set properly [7]. Thus, even when the I&Q inputs rotate, the cavity amplitude will be kept as a constant.

By using this method, the rf start-up of the cavities could be realized quickly and smoothly, without a long-time tuning of the mechanical tuner. Furthermore, because the input rf-frequency is always matched to the cavity resonance frequency during the rf start-up, the probability of the interlock due to reflection or VSWR will be reduced apparently.

This application is basically suitable for both the low-β and high-β sections of the J-PARC LINAC, and is planed to use mainly for all of the 972-MHz cavities.

SUMMARY

A lot of progresses have been successfully achieved in the LLRF FPGA control system for a more-convenient operation of the J-PARC LINAC with a high stability, especially for the 972-MHz high-β section of the J-PARC LINAC. Firstly automatically switching the beam loading compensation in accordance with the different beam operation mode has been realized. Furthermore, a chopped-beam compensation for the 972-MHz high-β section has also been carried out by the FPGA. Finally, besides the mechanical tuning method of rf cavities, an input rf-frequency tuning has also been performed by the FPGA control program.

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